SHRI VISHNU ENGINEERING COLLEGE FOR WOMEN:: BHIMAVARAM
(Autonomous)
DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

COURSE STRUCTURE (R22)
VLSI DESIGN

I Year -I Semester

S.No	Course Code	Name of the Course	L	P	C	I	E	T
1	PGEC1T0122	Analog IC Design	3	-	3	40	60	100
2	PGEC1T0222	Digital IC Design	3	-	3	40	60	100
3	PGEC1T0322	Linux & Scripting Languages	3	-	3	40	60	100
4	PGEC1T0422	VLSI Design	3	-	3	40	60	100
5	PGEC1T0522 PGEC1T0622 PGEC1T0722	**Elective-I** a. Digital System Design b. CPLD & FPGA Architectures c. Device Modeling	3	-	3	40	60	100
6	PGEC1P0822	Analog VLSI Lab	-	3	1.5	40	60	100
7	PGEC1P0922	Digital VLSI & Scripting Languages Lab	-	3	1.5	40	60	100
		Total	**15**	**6**	**18**	**280**	**420**	**700**

I Year -II Semester

S.No	Course Code	Name of the Course	L	P	C	I	E	T
1	PGEC2T0122	Physical Design	3	-	3	40	60	100
2	PGEC2T0222	Mixed Signal Circuit Design	3	-	3	40	60	100
3	PGEC2T0322	Low Power VLSI Design	3	-	3	40	60	100
4	PGEC2T0422 PGEC2T0522 PGEC2T0622	**Elective-II** a. Testing and Testability b. VLSI Signal Processing c. Optimization Techniques in VLSI Design	3	-	3	40	60	100
5	PGEC2T0722 PGEC2T0822 PGEC2T0922	**Elective-III** a. RF IC Design b. System on Chip Design c. Semiconductor Memory Design and Testing	3	-	3	40	60	100
6	PGEC2P1022	Mixed & RF VLSI Lab	-	3	1.5	40	60	100
7	PGEC2P1122	Physical Design Lab	-	3	1.5	40	60	100
		Total	**15**	**6**	**18**	**280**	**420**	**700**

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II Year -I Semester

S.No	Course Code	Name of the Course	L	P	C	I	E	T
1	PGEC3S0122	Comprehensive Viva	-	-	2	50	-	50
2		Project Work	-	-	14	-	-	-
		Total	**-**	**-**	**16**	**50**	**-**	**50**

II Year -II Semester

S.No	Course Code	Name of the Course	L	P	C	I	E	T
1	PGEC4S0122	Seminar	-	-	2	50	-	50
2	PGEC4J0222	Project Work	-	-	14	-	-	-
		Total	**-**	**-**	**16**	**50**	**-**	**50**

I YEAR I SEMESTER

ANALOG IC DESIGN

Subject Code : PGEC1T0122 **L T P C**

I Year/ I Semester **3 0 0 3**

Prerequisites

The student should have prior knowledge on

- Electronic circuits and Devices.
- Network Analysis
- Electronic Circuit Analysis
- Linear Integrated Circuits and Applications
- VLSI Design

Course Objectives: The objectives of this course is

1. To introduce the basics of MOSFET and its characteristics
2. To analyze the sma**l** signal analysis and large signal analysis for single stage amplifiers, differential amplifiers, current sources, current mirrors and frequency response of amplifiers.

SYLLABUS

UNIT I

MOS Devices and Modeling: The MOS Transistor, I-V characteristics of MOSFET, MOS Switch, MOS Diode, MOS Active Resistor, MOS Large-Signal Model, other Model Parameters, Sma**l**-Signal Model of MOSFET, Sub-threshold MOS Model, Integrated circuit Layout, SPICE Models.

UNIT II

CMOS Amplifiers: Common Source Amplifier configurations, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT III

Current Mirrors and Voltage References: Current Sinks and Sources, Basic Current Mirrors, Cascode Current Mirrors, Wilson Current Mirror, Current and Voltage References.

UNIT IV

CMOS Operational Amplifiers: Design of CMOS Op Amps, Compensation of Op Amps, Design of Two-Stage Op Amps, Power- Supply Rejection Ratio of Two Stage Op Amps, Cascode Op Amps, Measurement Techniques of OP Amp.

UNIT V

Comparators: Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete Time Comparators.

Course Outcomes: Upon completion of the course, students will be able to

Cos	Description	Bloom's Level
CO 1	Explain the small- and large-signal models of MOS transistors	II-Understanding
CO 2	Demonstrate the use of analog circuit analysis techniques to analyze the operation and behavior of various analog integrated circuits.	II-Understanding
CO 3	Analyze and design current mirror circuits	IV-Analyzing
CO 4	Analyze and design analog operational transconductance amplifiers	IV-Analyzing
CO 5	Design a two stage open loop comparator	VI-Creating

Mapping of Cos to Pos:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1	3		3								
CO 2	3	3	3	3							
CO 3	3	3	3	3					3		3
CO 4	3	3	3	3					3		
CO 5	3		3								

Text Books

T1. Phil ip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd edition, 2013.

T2. Behzad Razavi, "Analog CMOS Integrated Circuits", McGraw Hil, 2nd Edition 2017.

T3. Kenneth Martin, "Analog Integrated Circuit Design", Wiley Publications, 2nd Edition 2013.

Reference Books

R1. Paul. R. Gray, Paul. R. Hurst, Stephen H. Lewis & R. G. Meyer, "Analysis and Design of Analog Integrated Circuits", John Wiley Publications, 5th Edition 2010.

R2. Sedra and Smith, "Microelectronic Circuits", Oxford Publications, 6th Edition 2013.

DIGITAL IC DESIGN

Subject Code : PGEC1T0222 **L T P C**

I Year/ I Semester **3 0 0 3**

Prerequisites:

- VLSI design(UG level)
- Digital IC Applications (UG level)

Course Objective: The objectives of this course is

1. To introduce several aspects of digital integrated circuit design.
2. To give students the basic background to go through a complete digital design cycle: analysis, design, simulation, layout and verification.

SYLLABUS

UNIT I

MOS Design : Pseudo NMOS Logic–Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates , AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT III

Sequential MOS Logic Circuits: Behavior of bi-stable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT IV

Dynamic logic circuits: Basic principle, Voltage bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance dynamic CMOS circuits.

UNIT V

Semiconductor Memories : Types, RAM array organization, DRAM– Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.

Course Outcomes: Upon completion of the course, students will be able to

COs	Description	Bloom's Level
CO 1	Demonstrate the concepts of Pseudo NMOS, CMOS inverter logic.	II-Understanding
CO 2	Design Combinational Circuits using MOS logic circuits.	VI-Creating
CO 3	Design Sequential Circuits using MOS logic circuits.	VI-Creating
CO 4	Explain the high performance Dynamic Logic Circuits.	II-Understanding
CO 5	Summarize the Semiconductor memories-DRAM, SRAM, Flash Memory.	II-Understanding

Mapping of COs to POs:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1	3										
CO 2			3								
CO 3		3	3								
CO 4		3									
CO 5				3					3		

Text Books

T1. Ken Martin,"Digital Integrated Circuit Design", Oxford University Press, 2011.

T2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits Analysis and Design", TMH, 3rd Ed., 2011.

Reference Books

R1. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011

R2. Jan M. Rabaey, Anantha Chandrakasan, Borivoje Nikolic, " Digital Integrated Circuits – A Design Perspective", 2nd Ed., PHI.

LINUX & SCRIPTING LANGUAGES

Subject Code : PGEC1T0322 **L T P C**

I Year/ I Semester **3 0 0 3**

Prerequisites:

- Unix
- Any programming language(C/C++)

Course Objective: The objectives of this course is

- To master theory behind scripting and its relation to classic programming
- To design and implement one's own scripting language.

SYLLABUS

UNIT I

Introduction to Linux: File System of the Linux, General usage of Linux kernel & basic commands, Linux users and group, Permissions for file, directory and users, Searching a file & directory, zipping and unzipping concepts.

UNIT II

Linux Networking : Introduction to Networking in Linux, Network basics & tools, File transfer protocol in Linux, Network file system, Domain Naming Services, Dynamic hosting configuration Protocol & Network information Services

UNIT III

Introduction to Scripts and Scripting Characteristics and uses of scripting languages : Introduction to PERL, Names and values, Variables and assignment, Scalar expressions, Control structures, Built-in functions, Co**l**ections of Data, Working with arrays, Lists and hashes, Simple input and output, Strings, Patterns and regular expressions, Subroutines, Scripts with arguments

UNIT IV

Advanced PERL : Finer points of Looping, Subroutines, Using Pack and Unpack, Working with files, Navigating the file system, Type globs, Eval, References, Data structures, Packages, Libraries and modules, Objects, Objects and modules in action, Tied variables, Interfacing to the operating systems, Security issues.

UNIT V

TCL : The TCL phenomena, Philosophy, Structure, Syntax, Parser, Variables and data in TCL, Control flow, Data structures, Simple input/ output, Procedures Working with Strings, Patterns, Files and Pipes, Example code.

Course Outcomes: Upon completion of the course, students will be able to

Cos	Description	Bloom's Level
CO 1	Demonstrate Linux environment	II-Understanding
CO 2	Explain network establishment in Linux	II-Understanding
CO 3	Illustrate the Characteristics and uses of scripting languages	II-Understanding
CO 4	Develop programs using Advanced PERL	VI-Creating
CO 5	Develop programs using TCL	VI-Creating

Mapping of Cos to Pos:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1					3						
CO 2					3						
CO 3					3						
CO 4			3		3	3			3		
CO 5			3		3	3			3		

TEXT BOOKS:

T1. Red Hat Enterprise Linux 4: System Administration Guide Copyright 2005 Red Hat, Inc

T2. David Barron, "The World of Scripting Languages", Wiley Student Edition, 2010.

T3. Brent Welch, Ken Jones and Jeff Hobbs., "Practical Programming in Tcl and Tk", 4th edition.

T4. Larry Wall, Tom Christiansen, John Orwant, "Programming Perl", 3rd Edition, Oreilly publications

T5. Randal L, Schwartz Tom Phoenix, "Learning PERL", Oreilly publications

REFERENCE BOOKS

R1. Teach Yourself Perl 5 in 21 days by David Till.

R2. Tcl/Tk: A Developer's Guide- Clif Flynt, 2003, Morgan Kaufmann Series.

VLSI DESIGN

Subject Code : PGEC1T0422 **L T P C**

I Year/ I Semester **3 0 0 3**

Prerequisites

- VLSI design (UG level)
- Electronic Devices and Circuits(UG level)

Course Objective: The objectives of this course is

1. To give an overview of Silicon semiconductor technology process and the circuit design issues in the context of VLSI technology.
2. To introduce subsystem and architecture design.

SYLLABUS

UNIT I

IC fabrication process: Overview of semiconductor industry, Stages of Manufacturing, Crystal growth, Basic wafer fabrication operations, process yields, Semiconductor material preparation, Basic wafer fabrication operations, Y ield measurement, Contamination sources, Clean room construction, Oxidation and Photolithography.

UNIT II

Doping and Depositions: Metal**l**ization. Ten step patterning process, Photo resists, physical properties of photo resists, Storage and control of photo resists, photo masking process, Hard bake, develop inspect, Dry etching Wet etching, resist stripping, Diffusion process steps, deposition, Drive-in oxidation, Ion implantation-1, Ion implantation-2, CVD basics, CVD process steps, Low pressure CVD systems, Plasma enhanced CVD systems, Vapour phase epitaxy, molecular beam epitaxy.

UNIT III

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes. VLSI Design Issues: VLSI Design Flow, Design process, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations. Subsystem Design Processes: Some general considerations and an i**l**ustration of design processes, design of an ALU subsystem.

UNIT V

Architecture Design: Introduction, Register-Transfer design, high level synthesis, architectures for low power, architecture testing. Chip Design: Introduction and design methodologies.

Chip Input and Output Circuits, ESD Protection, Input Circuits, Output Circuits and noise, On-chip clock Generation and Distribution, Latch-up and its prevention

Course Outcomes: Upon completion of the course, students will be able to

COs	Description	Bloom's Level
CO 1	Demonstrate a clear understanding of IC fabrication process.	II-Understanding
CO 2	Summarise the doping and deposition concepts.	II-Understanding
CO 3	Demonstrate the MOS technologies and VLSI design Issues.	II-Understanding
CO 4	Illustrate sub system design process.	II-Understanding
CO 5	Develop various methologies in architectural design.	VI-Creating

Mapping of COs to POs:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1				3					3		
CO 2	3										
CO 3				3					3		
CO 4	3		3								
CO 5	3								3		3

Text Books

T1. Peter Van Zant, "Microchip fabrication", McGraw Hill, 1997

T2. K. Eshraghian, Douglas A. Pucknel, Sholeh Eshraghian, "Essentials of VLSI Circuits and Systems", 2005, PHI Publications.

T3. Wayne Wolf, "Modern VLSI Design", 3rd Ed., 1997, Pearson Education.

REFERENCE BOOKS:

R1. Randal L.Geiger, Phillip E.Allen, Noel R.Strader, "VLSI Design Technologies for Analog and Digital Circuits", TMH Publications, 2010.

R2. Dr.K.V.K.K.Prasad, Kattula Shyamala, "VLSI Design", Learning Solutions Inc., 2012.

R3. Ming-BO Lin, "Introduction to VLSI Systems: A Logic, Circuit and System Perspective", CRC Press, 2011.

R4. N.H.E Weste, K. Eshraghian, "Principles of CMOS VLSI Design", 2nd Edition, Addison Wesley

DIGITAL SYSTEM DESIGN

(ELECTIVE –I)

Subject Code : PGEC1T0522	**L**	**T**	**P**	**C**
I Year/ I Semester	**3**	**0**	**0**	**3**

Prerequisites

- Digital Logic Design (UG level)
- Digital IC Applications (UG level)

Course Objective: The objectives of this course is

1. To introduce several aspects of digital system concepts like PLAs.
2. To introduce the concepts & techniques of testing of digital circuits.

SYLLABUS

UNIT I

Minimization Procedures and CAMP Algorithm: Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholy within the given switching function or not, Introduction to cube based algorithms.

UNIT II

PLA Design, PLA Minimization and Folding Algorithms: Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, PLA design aspects, PLA minimization algorithm (IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT III

Design of Large Scale Digital Systems: Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design, ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.

UNIT IV

Fault Diagnosis in Combinational Circuits: Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method,

Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT V

Fault Diagnosis in Sequential Circuits: Fault detection and location in sequential circuits, circuit test approach, initial state identification, Homing experiments-synchronizing experiments, distinguishing experiment, adaptive distinguishing experiments, machine identification.

Course Outcomes: Upon completion of the course, students will be able to

COs	Description	Bloom's Level
CO 1	Make use of various minimization methods for minimizing the switching functions.	III-Applying
CO 2	Apply minimization and folding algorithms for PLA Design.	III-Applying
CO 3	Demonstrate various aspects in Large Scale Digital Systems design.	II-Understanding
CO 4	Apply the fault modeling concepts to digital circuits and generate the test patterns.	III-Applying
CO 5	Explain the concepts of fault diagnosis in Sequential Circuits.	II-Understanding

Mapping of COs to POs:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1	3	3									
CO 2	3	3									
CO 3			3						3		
CO 4		3	3								
CO 5		3	3	3					3		

Text Books:

T1. N. N. Biswas, "Logic Design Theory", PHI

T2. Z. Kohavi , "Switching and Finite Automata Theory", 2nd Edition, TMH, 2001

T3. P.K Lala, "Digital system Design using PLDs", Prentice Hal**l**, 1990

Reference Books

R1. Charles H. Roth, "Fundamentals of Logic Design", 5th Ed., Cengage Learning.

R2. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, "Digital Systems Testing and Testable Design", John Wiley & Sons Inc.

CPLD AND FPGA ARCHITECTURES

(ELECTIVE –I)

Subject Code : PGEC1T0622	**L**	**T**	**P**	**C**
I Year/ I Semester	**3**	**0**	**0**	**3**

Prerequisites.

- Digital Logic Design (UG level)
- Digital IC Applications (UG level)
- Microprocessors and Microcontrollers(UG level)

Course Objective:

1. Familiarization of various complex programmable logic devices of different families.
2. To study Field programmable gate arrays and realization techniques.
3. To study different case studies using one hot design methods.

SYLLABUS

UNIT I

Introduction to Programmable Logic Devices : Introduction, Simple Programmable Logic Devices–Read Only Memories, Programmable Logic Arrays, Programmable Array Logic, Programmable Logic Devices/Generic Array Logic; Complex Programmable Logic Devices– Architecture of Xilinx Cool Runner XCR3064XL CPLD, CPLD Implementation of a Parallel Adder with Accumulation.

UNIT II

Field Programmable Gate Arrays : Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/ O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs

UNIT III

SRAM Programmable FPGAs : Introduction, Programming Technology, Device Architecture, The Xilinx XC2000, XC3000 and XC4000 Architectures.

UNIT IV

Anti-Fuse Programmed FPGAs : Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures

UNIT V

Design Applications: General Design Issues, Counter Examples, A Fast Video Contro**l**er, A Position Tracker for a Robot Manipulator, A Fast DMA Contro**l**er, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.

Course Outcomes: Upon completion of the course, students will be able to

COs	Description	Bloom's Level
CO 1	Demonstrate various architectures and device technologies of PLDs and CPLDs.	II-Understanding
CO 2	**I**ustrate aspects of FPGA Architectures.	II-Understanding
CO 3	Explain SRAM Programmable FPGAs	II-Understanding
CO 4	Explain Anti-Fuse Programmed FPGAs	II-Understanding
CO 5	Analyze System level Design and their application for Combinational and Sequential Circuits	IV-Analyzing

Mapping of Cos to Pos:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1					3				3		
CO 2					3				3		
CO 3			3								3
CO 4			3								3
CO 5		3	3		3						

Text Books

T1. Stephen M. Trimberger, "Field Programmable Gate Array Technology", Springer International Edition.

T2. Charles H. Roth Jr, Lizy Kurian John, "Digital Systems Design", Cengage Learning

Reference Books

R1. John V. Oldfield, Richard C. Dorf, "Field Programmable Gate Arrays", Wiley India.

R2. Pak K. han/Samiha Mourad, "Digital Design Using Field Programmable Gate Arrays" - Pearson Low Price Edition.

R3. Ian Grout, "Digital Systems Design with FPGAs and CPLDs", Elsevier,

R4. Wayne Wolf, "FPGA based System Design", - Prentice Ha**l**

DEVICE MODELING

(ELECTIVE –I)

Subject Code : PGEC1T0722	**L**	**T**	**P**	**C**
I Year/I Semester	**3**	**0**	**0**	**3**

Prerequisites

- Solid State Physics

Course Objective: The objective of this course is

1. To provide students with a wide background and
2. To deal with advanced concepts in semiconductor electronic devices.

SYLLABUS

UNIT I

Basic Device Physics-I: Two Terminal MOS Structure: Flat-band voltage, Potential balance & charge balance, Effect of Gate-substrate voltage on surface condition, Inversion, Sma**l** signal capacitance; C-V Characteristics.

Three Terminal MOS Structure: Contacting the inversion layer, Body effect, Regions of inversion, Pinch-off voltage.

UNIT II

Basic Device Physics-II: Four Terminal MOS Transistor: Transistor regions of operation, general charge sheet models, regions of inversion in terms of terminal voltage, strong inversion, weak inversion, moderate inversion, interpolation models, effective mobility, temperature effects, breakdown p-channel MOSFET, enhancement and depletion type, model parameter values, model accuracy.

UNIT III

MOS Transistor with Ion-Implanted Channels: Enhancement of NMOS, Depletion NMOS, Enhancement PMOS. Sma**l** dimension effects: Channel length modulation, barrier lowering, two dimensional charge sharing and threshold voltage, punch-through, carrier velocity saturation, hot carrier effects, scaling, effects of surface and drain series resistance, effects due to thin oxides and high doping. Sub threshold regions, Short channel effects.

UNIT IV

MOS Transistor in Dynamic Operation: Large Signal modeling: Quasi static operation, Terminal currents in Quasi static operation, Evaluation of Charges in Quasi

static operation, Transit time under DC conditions, Limitations of Quasi static Model, Non Quasi static Analysis.

UNIT V

Small Signal Modeling for Low, Medium And High Frequencies: low, Medium frequency sma**l** signal model for the intrinsic part, Sma**l** signal model for Extrinsic Part, A complete Quasi static Model, Y-Parameter models, Non Quasi static Models.

Course Outcomes: Upon completion of the course, students will be able to

COs	Description	Bloom's Level
CO 1	Extend in depth knowledge in various characteristics of MOS Transistors.	II-Understanding
CO 2	Analyze complex MOS device structures.	IV-Analyzing
CO 3	Solve engineering problems with wide range of solutions in different MOSFET technologies.	III-Applying
CO 4	Identify the characteristics of MOSFET in dynamic operation	III-Applying
CO 5	Apply appropriate techniques, resources and tools to engineering activities in modeling MOS structures.	III-Applying

Mapping of COs to POs:

POs	1	2	3	4	5	6	7	8	9	10	11
CO 1	3			3					3		
CO 2	3			3					3		
CO 3	3			3					3		
CO 4				3					3		
CO 5	3			3	3				3		

Text Books

T1. Y.Tsividis, "Operations and Modeling of the MOS Transistor", Oxford university Press,3rd edition, 2012.

Reference Books

R1. Trond Ytterdal, Yuhua Cheng and Tor Fjeldly "Device Modeling for Analog and RF CMOS Circuit Design" Wiley Publication, 2003.

R2. Donald A Neamen and Dhrubes Biswas "Semiconductor Physics and Devices" Special Indian Edition, 4 th edition, 2012.

R3. M.S. Tyagi, "Introduction to Semiconductor Materials and Devices", Wiley, 2008.

R4. Ben G Streetman, "Solid State Electronic Devices", 6th Edition, Pearson Prentice-Hall, 2009.

ANALOG VLSI LAB

Subject Code : PGEC1P0822 **L T P C**

I Year/ I Semester **0 0 3 1.5**

Prerequisites

- Analog IC design
- VLSI Design

Laboratary Objective: The objective of this lab is

- to set up an own design library
- to familiarize with a full custom IC design flow.

Experiments

1. Introduction to Cadence Virtuoso full custom design flow
2. Characteristics of MOS transistors
3. Design of inverter in CMOS configuration.
4. Single transistor amplifier: Ideal current source, PMOS current source, NMOS saturated load, degenerative resistor
5. Cascode amplifier: Ideal current source, PMOS current source.
6. Current sinks: Basic current sink, Current sink with negative feedback
7. Current sources: Basic current source, Current source with negative feedback, Bootstrap current source.
8. Current mirrors: Basic current mirror, Cascode current mirror.
9. Differential amplifier using current mirror.

Laboratary Outcomes: Upon completion of the Laboratary, students will be able to

LOs	Description	Bloom's Level
LO 1	Develop pre-layout simulations using Spectre.	III-Applying
LO 2	Apply Layout specific rules using Cadence virtuoso.	III-Applying
LO 3	Compile post layout simulation by extracting the net list.	VI-Creating
LO 4	Experiment with complete analog circuit on silicon using state-of-the art.	III-Applying

Mapping of LOs to POs:

POs	1	2	3	4	5	6	7	8	9	10	11
LO 1				3	3						
LO 2		3		3	3				3		
LO 3				3	3						
LO 4		3		3	3				3		

DIGITAL VLSI & SCRIPTING LANGUAGES LAB

Subject Code : PGEC1P0922 **L T P C**

I Year/ I Semester **0 0 3 1.5**

Prerequisites

- Digital IC design
- VLSI Design

Laboratary Objective: The main objective of this lab is

1. To enhance the student skil in HDL programming to design digital circuits that can be simulated, synthesized using Xilinx/Cadence tools and can be implemented on FPGA boards

List of Experiments

Modeling and Functional Simulation of the folowing digital circuits (with Xilinx/Cadence Encounter) using Verilog Hardware Description Languages.

1. **Part – I Combinational Logic:** Basic Gates, Multiplexer, Comparator, Adder/ Subs tractor, Multipliers, Decoders, Address decoders, parity generator, ALU
2. **Part – II Sequential Logic:** D-Latch, D-Flip Flop, JK-Flip Flop, Registers, Ripple Counters, Synchronous Counters, Shift Registers (serial-to-paralel, paralel-to-serial), Cyclic Encoder / Decoder.
3. **Part – III Memories and State Machines:** Read Only Memory (ROM), Random Access Memory (RAM), Mealy State Machine, Moore State Machine, Arithmetic Multipliers using FSMs
4. **Part – IV FPGA System Design:** Demonstration of FPGA Boards, Demonstration of Digital design using FPGAs
5. **Part-V Scripting languages:** Perl script for various digital circuits

Laboratary Outcomes: Upon completion of the Laboratary, students wil be able to

LOs	Description	Bloom's Level
LO 1	Design & Verify the functionality of digital systems using HDL.	VI-Creating
LO 2	Show timing simulation for digital systems.	II-Understanding
LO 3	Experiment with digital circuits using FPGA.	III-Applying
LO 4	Model the digital circuits using scripting languages.	III-Applying

Mapping of LOs to Pos:

POs	1	2	3	4	5	6	7	8	9	10	11
LO 1				3	3				3		
LO 2		3		3	3				3		
LO 3		3		3	3				3		
LO 4					3				3		

I YEAR II SEMESTER

PHYSICAL DESIGN

Subject Code : PGEC2T0122 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites

- VLSI design (UG Level)

Course Objective: The course objectives of the subject are

1. To provide basic knowledge of VLSI design and
2. To know about various methodologies using several algorithms

SYLLABUS

UNIT I

VLSI Physical Design Automation : VLSI Design Cycle, New Trends in VLSI Design Cycle, Physical Design Cycle, New Trends in Physical Design Cycle, Design Styles, System Packaging Styles.

UNIT II

Graph Theory and Computational Geometry: Basic Terminology, Basic Graph Algorithms :Graph Search Algorithms- Depth-First Search, Breadth-First Search. Spanning Tree Algorithms- Kruskal's Algorithm. Shortest Path Algorithms- Single Pair Shortest Path, All Pairs Shortest Paths Computational Geometry Algorithms - Line Sweep Method, Extended Line Sweep Method.

UNIT III : Partitioning, Floor Planning, Pin Assignment and Placement

Partitioning – Problem formulation, Classification of Partitioning algorithms-Kernighan-Lin Algorithm, Extensions of Kernighan-Lin algorithm ,Simulated Annealing and Evolution, Metric a**l**location method.

Floor Planning – Problem formulation, Classification of floor planning algorithms - constraint based floor planning, Rectangular Dualization.

Pin Assignment – Problem formulation, Classification of pin assignment algorithms-General and channel Pin assignments.

Placement – Problem formulation, Classification of placement algorithms- Partitioning based placement algorithms;

UNIT IV : Global Routing and Detailed Routing:

Global Routing – Problem formulation, Classification of global routing algorithms-Maze routing algorithms, Line-Probe Algorithms, Shortest Path Based Algorithms, Steiner Tree based Algorithms

Detailed Routing – Problem formulation, Classification of routing algorithms- Single layer routing algorithms

UNIT V

Physical Design Automation of FPGAs and MCMs: FPGA Technologies-Physical Design cycle for FPGAs, Partitioning, Routing – Routing Algorithm for the Non-Segmented model, Routing Algorithms for the Segmented Model. MCM Technologies-Introduction to MCM Technologies, MCM Physical Design Cycle

Course Outcomes : At the end of the course, the student should be able to:

COs	Course outcomes	Bloom's level
CO 1.	Demonstrate about various steps in VLSI Design cycle	II Understanding
CO 2.	Formulate CAD design using algorithmic paradigms	VI Creating
CO 3.	Apply various algorithms for floor planning, routing and Placement	III Applying
CO 4.	Analyze physical design including partitioning, floor planning, placement and routing	IV Analyzing
CO 5.	Summarize physical design automation for FPGA, CPLD & MCM's	II Understanding

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1				3							
CO 2			3	3	3						
CO 3		3	3	3	3		3		3		3
CO 4				3	3		3		3		3
CO 5				3							

Text Books

T1. Naveed Shervani, "Algorithms for VLSI Physical Design Automation", 3rd Edition, 2005, Springer International Edition.

T2. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", TMH, 3rd Edition, 2011.

Reference Books

R1. Sadiq M Sait, Habib Youssef, "VLSI Physical Design Automation-Theory and Practice" World Scientific.

R2. S. H. Gerez, "Algorithms for VLSI Design Automation", Wiley student Edition, John Wiley and Sons (Asia) Pvt. Ltd. 1999,

MIXED SIGNAL CIRCUIT DESIGN

Subject Code : PGEC2T0222 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites

The student should have prior knowledge on

- Linear Integrated Circuits and Applications
- Analog IC Design

Course Objective: The objectives of this course are

1. To introduce the basics of Switched Capacitor circuits
2. To design Phase Locked Loops, Digital to Analog converters, Analog to Digital converters and higher order sampling converters

SYLLABUS

UNIT I

Switched Capacitor Circuits: Introduction to Switched Capacitor circuits- basic building blocks, Operation and Analysis, Non-ideal effects in switched capacitor circuits, Switched capacitor integrators first order filters, Switch sharing, Biquad filters.

UNIT II

Phased Lock Loop (PLL): Basic PLL topology, Dynamics of simple PLL, Charge pump PLLs Lock acquisition, Phase/Frequency detector and charge pump, Basic charge pump PLL, Non ideal effects in PLLs- PFD/CP non-idealities, Jitter in PLLs, Delay locked loops, applications.

UNIT III

Data Converters: Fundamentals DC and dynamic specifications, Quantization noise, Nyquist rate D/A converters- Decoder based converters, Binary-Scaled converters, Thermometer-code converters, Hybrid converters.

UNIT IV

Nyquist Rate A/D Converters: Successive approximation converters, Flash converter, Two step A/D converters, Interpolating A/D converters, Folding A/D converters, Pipelined A/D converters, Time interleaved converters.

UNIT V

Over sampling Converters: Noise shaping modulators, Decimating filters and interpolating filters, Higher order modulators, Delta sigma modulators with multi bit quantizers, Delta sigma D/A.

Course Outcomes:

At the end of the course, the students should be able to

COs	Course outcomes	Bloom's level
CO 1.	Demonstrate and design Switched Capacitor Circuits	II Understanding
CO 2.	Explain the building blocks of PLL and its operation	II Understanding
CO 3.	Solve engineering problems related to D/A Converters	III Applying
CO 4.	Apply appropriate techniques, and tools in development of A/D Converters	III Applying
CO 5.	Analyze appropriate techniques and Design Over sampling converters	IV Analyzing

Mapping of Cos to Pos :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1	3		3	3	3		3		3		
CO 2				3	3		3				
CO 3			3	3	3		3		3		3
CO 4			3	3	3		3		3		3
CO 5			3	3	3		3		3		3

Text Books

T1. Kenneth Martin, "Analog Integrated Circuit Design", Wiley Publications, 2nd Edition 2013.

T2. Phi**l**ip E. Allen, Douglas R. Holberg, "CMOS Analog Circuit Design", Oxford University Press, 3rd edition, 2013.

T3. Behzad Razavi, "Analog CMOS Integrated Circuits", McGraw Hi**l**, 2nd Edn 2017.

Reference Books

R1. M. Gustavsson, J. Wikner, and N. Tan. Kluwer, "CMOS Data Converters for Communication", Academic Publishers, 1st Edition 2000.

R2. Behzad Razavi, "Principles of Data Conversion System Design", Wiley Inter science, 1st Edition 1994.

R3. R. Jacob Baker, "CMOS Mixed-Signal Circuit Design", Wiley Inter science, IEEE press, 2nd Edition, 2008.

R4. Franco Maloberti, "Data Converters"=, Springer Publications, 2nd Edition, 2007.

LOW POWER VLSI DESIGN

Subject Code : PGEC2T0322 **L T P C**
I Year/ II Semester **3 0 0 3**
Prerequisites

- VLSI Design

Course Objective: The course objectives of the course are

1. To provide basic knowledge of low voltage device modeling
2. To provide overview of low voltage, low power VLSI CMOS circuit design

SYLLABUS

UNIT I

Fundamentals of Low Power VLSI Design : Need for Low Power Circuit Design, Sources of Power Dissipation – Switching Power Dissipation, Short Circuit Power Dissipation, Leakage Power Dissipation, Glitching Power Dissipation, Short Channel Effects –Drain Induced Barrier Lowering and Punch Through, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Electron Effect.

UNIT II

Low Power Design Approaches: Low-Power Design through Voltage Scaling – VTCMOS circuits, MTCMOS circuits, Architectural Level Approach – Pipelining and Para**l**el Processing Approaches. Switched Capacitance Minimization Approaches System Level Measures, Circuit Level Measures, Mask level Measures. Adiabatic Logic Circuits: Adiabatic Charging, Adiabatic Amplification, Adiabatic Logic Gates, Pulsed Power Supply, Stepwise Charging Circuits Low-Power.

UNIT III

Low-Voltage Low-Power Adders: Introduction, Standard Adder Ce **l**s, CMOS Adder's Architectures – Ripple Carry Adders, Carry Look-Ahead Adders, Carry Select Adders, Carry Save Adders, Low-Voltage Low- Power Design Techniques –Trends of Technology and Power Supply Voltage, Low-Voltage Low-Power Logic Styles.

UNIT IV

Low-Voltage Low-Power Multipliers: Introduction, Overview of Multiplication, Types of Multiplier Architectures, Braun Multiplier, Baugh-Wooley Multiplier, Booth Multiplier, Introduction to Wa**l**ace Tree Multiplier.

UNIT V

Low-Voltage Low-Power Memories: Basics of ROM, Low-Power ROM Technology, Future Trend and Development of ROMs, Basics of SRAM, Memory Ce**l**, Pre charge and

Equalization Circuit, Low-Power SRAM Technologies, Basics of DRAM, Self-Refresh Circuit, Future Trend and Development of DRAM. VLSI, VLSI Design, VLSI System Design, VLSI & MICRO ELECTRONICS

Course Outcomes : At the end of the course, the students should be able to

COs	Course outcomes	Bloom's level
CO 1	Demonstrate in depth knowledge in the limitations of low power design and different sources of power dissipation	II Understanding
CO 2	Acquire the knowledge in various low power design approaches and techniques	III Applying
CO 3	Analyze and design various types of low power adders	IV Analyzing
CO 4	Apply the different low power techniques for designing multipliers	III Applying
CO 5	Apply the different low power techniques for designing multipliers	III Applying

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1	3			3			3		3		3
CO 2			3	3	3		3		3		
CO 3		3	3	3	3		3		3		
CO 4		3	3	3	3		3		3		
CO 5							3		3		3

Text Books

T1. Sung-Mo Kang, Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design",TMH, 2011.

T2. Kiat-Seng Yeo, Kaushik Roy, "Low-Voltage, Low-Power VLSI Subsystems", TMH Professional Engineering.

T3. Pal, Ajit, "Low-Power VLSI Circuits and Systems", Springer,2015

Reference Books:

R1. Anantha Chandrakasan, "Low Power CMOS Design", IEEE Press/Wiley International, 1998.

R2. Kaushik Roy, Sharat C. Prasad, "Low Power CMOS VLSI Circuit Design", John Wiley & Sons, 2000.

R3. Gary K. Yeap, "Practical Low Power Digital VLSI Design", Kluwer Academic Press, 2002.

R4. A. Be**l**amour, M. I. Elamasri, "Low Power CMOS VLSI Circuit Design", Kluwer Academic Press, 1995.

TESTING AND TESTABILITY
(ELECTIVE –II)

Subject Code : PGEC2T0422 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites
- VLSI Design

Course Objective: The course objectives of the course are
1. To provide the basics of testing techniques for VLSI circuits.

SYLLABUS

UNIT I

INTRODUCTION TO TEST AND DESIGN FOR TESTABILITY (DFT) FUNDAMENTALS: Modeling: Modeling Digital Circuits at Logic Level, Register Level and Structural Models. Levels of Modeling. Logic Simulation: Types of Simulation, Delay Models, Element Evaluation, Hazard Detection, Gate Level Event Driven Simulation

UNIT II

FAULT MODELING: Logic Fault Models, Fault Detection and Redundancy, Fault Equivalence and Fault Location. Single Stuck and Multiple Stuck – Fault Models. Fault Simulation Applications, General Techniques for Combinational Circuits

TESTING FOR SINGLE STUCK FAULTS(SSF): Automated Test Pattern Generation (ATPG/ATG) For SSFs In Combinational and Sequential Circuits, Functional Testing With Specific Fault Models. Vector Simulation – ATPG Vectors, Formats, Compaction and Compression, Selecting ATPG Tool.

UNIT III

DESIGN FOR TESTABILITY: Testability Trade-Offs, Techniques. Scan Architectures and Testing – Contro**l**ability and Absorbability, Generic Boundary Scan, Fu**l**l Integrated Scan, Storage Ce**l**s for Scan Design. Board Level and System Level DFT Approaches. Boundary Scans Standards. Compression Techniques – Different Techniques, Syndrome Test andSignature Analysis.

UNIT IV

BUILT-IN SELF-TEST (BIST): BIST Concepts and Test Pattern Generation. Specific BIST Architectures – CSBL, BEST, RTS, LOCST, STUMPS, CBIST, CEBS, RTD, SST, CATS, CSTP, BILBO. Brief Ideas on Some Advanced BIST Concepts and Design for Self-Test at Board Level.

UNIT V

MEMORY BIST (MBIST): Memory Test Architectures and Techniques – Introduction to Memory Test, Types of Memories and Integration, Embedded Memory Testing Model. Memory Test Requirements for MBIST.

Course Outcomes: At the end of the course the student should be able to

COs	Course outcomes	Bloom's level
CO 1.	Model the digital circuits at logic level and register level	III Applying
CO 2.	Identify the problems associated with testing of semiconductor circuits at earlier design levels so as to significantly reduce the testing costs	III Applying
CO 3.	Analyze various Trade-Offs and Techniques for Testability	IV Analyzing
CO 4.	Explain the concepts of built-in-self-test	II Understanding
CO 5.	Illustrate the Memory Test Architectures and Techniques	II Understanding

Mapping of Cos to Pos :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1	3			3							
CO 2				3					3		
CO 3				3					3		
CO 4				3					3		
CO 5				3							

Text Books

T1. Miron Abramovici, Melvin A. Breur, Arthur D.Friedman, "Digital Systems Testing and Testable Design", Jaico Publishing House, 2001.

Reference Books

R1. Robert J.Feugate, Jr., Steven M.Mentyn, "Introduction to VLSI Testing", PHl, Englehood Cliffs, 1998.

R2. Alfred Crouch, "Design for Test for Digital ICs & Embedded Core Systems", Prentice Hall.

VLSI SIGNAL PROCESSING
(ELECTIVE –II)

Subject Code : PGEC2T0522 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites

- Digital signal processing
- VLSI design

Course Objective: The course objectives of the course are

1. To Design the DSP architecture using IIR and FIR filters by applying parallel processing, retiming, folding and un folding techniques.

SYLLABUS

UNIT I

Introduction to DSP Typical DSP algorithms: DSP algorithms benefits, Representation of DSP algorithms Pipelining and Parallel Processing Introduction, Pipelining of FIR Digital filters, Parallel Processing, Pipelining and Parallel Processing for Low Power Retiming Introduction–Definitions and Properties – Solving System of Inequalities – Retiming Techniques

UNIT II

Folding: Introduction, Folding Transform, Register minimization Techniques, Register minimization in folded architectures, Folding of multirate systems.

Unfolding: Introduction, An Algorithm for Unfolding, Properties of Unfolding, critical Path, Unfolding and Retiming, Applications of Unfolding

UNIT III

Systolic Architecture Design Introduction: Systolic Array Design Methodology, FIR Systolic Arrays – Selection of Scheduling Vector, Matrix Multiplication and 2D Systolic Array Design, Systolic Design for Space Representations contain Delays.

UNIT IV

Fast Convolution Introduction: Cook-Toom Algorithm, Winograd algorithm, Iterated Convolution, Cyclic Convolution, Design of Fast Convolution algorithm by Inspection,

UNIT V

Low Power Design Scaling Vs Power Consumption: Power Analysis, Power Reduction techniques – Power Estimation Approaches Programmable DSP: Evaluation of Programmable Digital Signal Processors, DSP Processors for Mobile and Wireless Communications, Processors for Multimedia Signal Processing.

Course Outcomes

At the end of the course the student should be able to

COs	Course outcomes	Bloom's level
CO 1	Design architectures for DSP algorithms	VI Creating
CO 2	Improve the speed of digital system through transformation techniques	VI Creating
CO 3	Minimize the design in terms of area,delay and power	VI Creating
CO 4	Explain pipeline based architectures in the design FIR and IIR systems	II Understanding
CO 5	Demonstrate clocking issues and asynchronous system	II Understanding

Mapping of Cos to Pos :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1	3		3	3	3		3				3
CO 2			3	3	3		3				
CO 3	3	3		3	3		3				3
CO 4	3	3		3			3		3		
CO 5				3					3		

Text Books

T1. Keshab K. Parhi, "VLSI Digital Signal Processing- System Design and Implementation", Wiley Inter Science, 1998.

T2. Kung S. Y, H. J. ,T.Kailath, "VLSI and Modern Signal Processing", PHI, 1985.

Reference Books

R1. Jose E. France, Yannis Tsividis, "Design of Analog and Digital VLSI Circuits for Telecommunications and Signal Processing", Prentice Hall, 1994

R2. Medisetti V. K, "VLSI Digital Signal Processing", IEEE Press, USA, 1995.

OPTIMIZATION TECHNIQUES IN VLSI DESIGN

(ELECTIVE –II)

Subject Code : PGEC2T0622 **L T P C**

I Year/ II Semester **3 0 0 3**

Pre requisites

- Basic knowledge of electronic design automation (EDA)
- Digital design

Course Objective: The course objectives of the course are

1. To learn digital VLSI design flow, High-level Synthesis, logic synthesis, physical synthesis and apply these levels to optimization
2. To observe its Impact of compiler optimization on hardware synthesis.

SYLLABUS

UNIT-I

Statistical Modeling : Modeling sources of variations, Monte Carlo techniques, Process variation modeling- Pelgrom's model, Principle component based modeling, Quad tree based modeling, Performance modeling- Response surface methodology, delay modeling, interconnect delay models.

UNIT-II

Statistical Performance, Power and Yield Analysis: Statistical timing analysis, parameter space techniques, Bayesian networks Leakage models, High level statistical analysis, Gate level statistical analysis, dynamic power, leakage power, temperature and power supply variations, High level yield estimation and gate level yield estimation.

UNIT-III

Convex Optimization: Convex sets, convex functions, geometric programming, trade-off and sensitivity analysis, Generalized geometric programming, geometric programming applied to digital circuit gate sizing, Floor planning, wire sizing, Approximation and fitting- Monomial fitting, Maxmonomial fitting, Polynomial fitting.

UNIT-IV

Genetic Algorithm Introduction: GA Technology-Steady State Algorithm-Fitness Scaling-Inversion GA for VLSI Design, Layout and Test automation- partitioning-automatic placement, routing technology, Mapping for FPGA- Automatic test generation- Partitioning algorithm Taxonomy-Multi-way Partitioning Hybrid genetic-

encoding-local Improvement- WDFR Comparison of CAS-Standard cell placement- GASP algorithm-unified algorithm.

UNIT-V

GA Routing Procedures and Power Estimation: Global routing-FPGA technology mapping-circuit generation-test generation in a GA frame work-test generation procedures, Power estimation-application of GA Standard cell placement-GA for ATG-problem encoding- fitness function-GA Vs Conventional algorithm.

Course Outcomes : At the end of the course the student should be able to

COs	Course outcomes	Bloom's level
CO 1	Model the process variation, delay variations, interconnects delay model parameters using Monte Carlo techniques	III Applying
CO 2	Compare the performance and power analysis for temperature and power supply variations	IV Analyzing
CO 3	Apply convex optimization for gate sizing, floor planning, wire sizing	III Applying
CO 4	Apply the genetic algorithm for layout, placement of cells and Routing between the cells	III Applying
CO 5	Evaluate the power estimation using genetic algorithm	V Evaluating

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1	3			3	3						
CO 2		3		3	3						3
CO 3	3		3	3	3		3				3
CO 4	3		3	3	3						3
CO 5		3	3	3	3		3				

Text Books

T1. Ashish Srivastava, Dennis Sylvester, David Blaauw, "Statistical Analysis and Optimization for VLSI: Timing and Power", Springer, 2005.

T2. Pinaki Mazumder, E.Mrudnick, "Genetic Algorithm for VLSI Design, Layout and Test Automation", Prentice Hall, 1998.

Reference Books

R1. Stephen Boyd, Lieven Vandenberg he "Convex Optimization", Cambridge University Press, 2004.

RF IC DESIGN
(ELECTIVE –III)

Subject Code : PGEC2T0722 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites

- Analog IC Design

Course Objective: The course objectives of the course are

1. To introduce the principles of RF communication circuits and apply the techniques for the design of RF integrated circuit (RF IC's).

SYLLABUS

UNIT I

Basic Concepts in RF Design: Introduction to RF Design, Units in RF design, Time Variance and Nonlinearity, Effects of nonlinearity, random processes and Noise, Definitions of sensitivity and dynamic range, Passive impedance transformation, Scattering parameters.

UNIT II

Transceiver Architectures: General considerations, Receiver Architectures-Basic Heterodyne receivers, Modern heterodyne receivers, Direct conversion receivers, Image-Reject receivers, Low-IF receivers. Transmitter Architectures -Direct Conversion transmitters, Modern direct conversion Transmitters, Heterodyne Transmitters, Other Transmitter Architectures.

UNIT III

LNA and Mixers: General considerations, Problem of input matching, Low Noise Amplifiers design in various topologies, Gain Switching, Band Switching.

Mixers-General considerations, Passive down conversion mixers, Active down conversion mixers, Up conversion mixers.

UNIT IV

Oscillators: Performance parameters, Basic principles, Cross coupled oscillator, Three point oscillators, Voltage Controlled Oscillators, LC VCOs with wide tuning range, phase noise, Mathematical model of VCOS, Quadrature Oscillators.

UNIT V

Power Amplifier: General considerations, Classification of power amplifiers, High-Efficiency power amplifiers, Cascode output stages, Large signal impedance matching, Linearization techniques.

Course Outcomes: At the end of the course the students should be able to

COs	Course outcomes	Bloom's level
CO 1	Demonstrate in-depth knowledge in Radio Frequency Integrated Circuits	II Understanding
CO 2	Analyze transceiver architecture in Radio Frequency Integrated Circuits	IV Analyzing
CO 3	Design LNA and Mixers in Radio Frequency Integrated circuits	VI Creating
CO 4	Explain the performance of oscillator circuits	II Understanding
CO 5	Analyze and design high efficiency power amplifier	IV Analyzing

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1				3			3		3		
CO 2	3	3	3	3	3		3		3		3
CO 3		3	3	3	3		3				3
CO 4				3			3				
CO 5			3	3	3		3				3

TEXT BOOKS:

T1. B.Razavi, "RF Microelectronics", Prentice-Hall PTR, 2nd Edition, 1998.

REFERENCE BOOKS:

R1. T.H.Lee, "The Design of CMOS Radio-Frequency Integrated Circuits", Cambridge University Press, 2nd, 1998.

R2. R.Jacob Baker, Harry W.Li, D.E. Boyce, "CMOS Circuit Design, Layout and Simulation", Prentice-Hall of India, 1998.

SYSTEM ON CHIP DESIGN
(ELECTIVE –III)

Subject Code : PGEC2T0822 **L T P C**
I Year/ II Semester **3 0 0 3**

Prerequisites

- Embedded real-time system design and hardware/software interfacing
- Digital hardware design and hardware description languages
- It is helpful to have some basic knowledge of communication systems.

Course Objective: The course objectives of the course are

1. To design processor based system on chip
2. To design the memory based system on chip

SYLLABUS

UNIT I

Introduction to the System Approach: System Architecture, Components of the system, Hardware & Software, Processor Architectures, Memory and Addressing. System level interconnection, approach for SOC Design, System Architecture and Complexity.

UNIT II

Processors : Introduction, Processor Selection for SOC, Basic concepts in Processor Architecture, Basic concepts in Processor Micro Architecture, Basic elements in Instruction handling. Buffers: minimizing Pipeline Delays, Branches, More Robust Processors, Vector Processors and Vector Instructions extensions, VLIW Processors, Superscalar Processors.

UNIT III

Memory Design for SOC : Overview of SOC external memory, Internal Memory, Size, Scratchpads and Cache memory, Cache Organization, Cache data, Write Policies, Strategies for line replacement at miss time.

Types of Cache, Split – I, and D – Caches, Multilevel Caches, Virtual to real translation , SOC Memory System, Models of Simple Processor – memory interaction.

UNIT IV

Interconnect Customization and Configuration : Inter Connect Architectures, Bus: Basic Architectures, SOC Standard Buses , Analytic Bus Models, Using the Bus model, Effects of Bus transactions and contention time. SOC Customization: An overview, Customizing Instruction Processor, Reconfiguration Technologies, Mapping

design onto Reconfigurable devices, Instance-Specific design, Customizable Soft Processor, Reconfiguration - overhead analysis and trade-off analysis on reconfigurable Para**l**elism.

UNIT V

Application Studies / Case Studies: SOC Design approach, AES algorithms, Design and evaluation, Image compression – JPEG compression.

Course Outcomes: At the end of the course the student should be able to

COs	Course outcomes	Bloom's level
CO 1	Demonstrate the abstraction in Hardware, SOC of ARM Processor	II. Understanding
CO 2	Evaluate and analyze system on chip RISC Machine, three and five stage Pipeline	V. Evaluating
CO 3	Explain Memory Design for SOC	II. Understanding
CO 4	Develop the Interconnect Customization and Configuration	III. Applying
CO 5	Explain the SOC design approaches and AES algorithm	II. Understanding

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1				3			3		3		
CO 2	3	3	3	3			3		3		
CO 3				3			3		3		
CO 4			3	3	3		3				
CO 5				3			3				

Text Books

T1. Michael J. Flynn and Wayne Luk, "Computer System Design System-on-Chip", Wiely India Pvt. Ltd.

T2. Steve Furber, "ARM System on Chip Architecture", 2nd Ed., Addison Wesley Professional, 2000.

Reference Books

R1. Ricardo Reis, "Design of System on a Chip: Devices and Components", 1st Edition, Springer, 2004

R2. Prakash Rashinkar, Peter Paterson and Leena Singh L, "System on Chip Verification – Methodologies and Techniques", 2001.

SEMICONDUCTOR MEMORY DESIGN AND TESTING

(ELECTIVE –III)

Subject Code : PGEC2T0922 **L T P C**

I Year/ II Semester **3 0 0 3**

Pre Requisites

- CMOS Digital IC design
- Design for testability

Course objective : The objective of this course is

1. To acquire knowledge about different types of semiconductor memories.
2. To study about architecture and operations of different semiconductor memories.
3. To comprehend the low power design techniques and methodologies

SYLLABUS

UNIT-I

Random Access Memory Technologies: SRAM – SRAM Ce**l** structures, MOS SRAM Architecture, MOS SRAM ce**l** and peripheral circuit operation, Bipolar SRAM technologies, SOI technology, Advanced SRAM architectures and technologies, Application specific SRAMs, DRAM – DRAM technology development, CMOS DRAM, DRAM ce**l** theory and advanced ce**l** structures, BICMOS DRAM, soft error failure in DRAM, Advanced DRAM design and architecture, Application specific DRAM.

UNIT-II

Non-volatile Memories: Masked ROMs, High density ROM, PROM, Bipolar ROM, CMOS PROMS, EPROM, Floating gate EPROM ce**l**, One time programmable EPROM, EEPROM, EEPROM technology and architecture, Non-volatile SRAM, Flash Memories (EPROM or EEPROM), advanced Flash memory architecture

UNIT-III

Memory Fault Modeling Testing and Memory Design for Testability and Fault Tolerance: RAM fault modeling, Electrical testing, Pseudo Random testing, Megabit DRAM Testing, non-volatile memory modeling and testing, IDDQ fault modeling and testing, Application specific memory testing, RAM fault modeling, BIST techniques for memory

UNIT-IV

Semiconductor Memory Reliability and Radiation Effects: General reliability issues RAM failure modes and mechanism, Non-volatile memory reliability, reliability modeling and failure rate prediction, Design for Reliability, Reliability Test Structures, Reliability Screening and qualification, Radiation effects, Single Event Phenomenon (SEP), Radiation Hardening techniques, Radiation Hardening Process and Design Issues,

Radiation Hardened Memory characteristics, Radiation Hardness Assurance and Testing, Radiation Dosimetry, Water Level Radiation Testing and Test structures

UNIT-V

Advanced Memory Technologies and High-density Memory Packing Technologies:

Ferroelectric RAMs (FRAMs), GaAs FRAMs, Analog memories, magneto resistive RAMs (MRAMs), Experimental memory devices, Memory Hybrids and MCMs (2D), Memory Stacks and MCMs (3D), Memory MCM testing and reliability issues, Memory cards, High Density Memory Packaging Future Directions.

Course outcomes: At the end of this course students should be able to

COs	Course outcomes	Bloom's level
CO 1	Analyze the different types of RAM, ROM designs	IV. Analyzing
CO 2	Design the RAM, ROM architecture and interconnects.	VI. Creating
CO 3	Analyze different memory testing methods and design for testability	IV. Analyzing
CO 4	Identify the new developments in semiconductor memory design	III. Applying
CO 5	Explain about various Advanced and High-density Memory Technologies	II. Understanding

Mapping of COs to POs :

POs	PO1	PO2	PO3	PO4	PO5	PO6	PO7	PO8	PO9	PO10	PO11
CO 1				3							
CO 2			3	3	3						
CO 3		3	3	3	3				3		
CO 4				3					3		3
CO 5				3					3		3

Text Books

T1. Ashok K. Sharma, "Semiconductor Memories Technology", Wiley, 2002.

T2. Ashok K. Sharma, "Advanced Semiconductor Memories – Architecture, Design and Applications", Wiley, 2002

T3. Chenming C Hu, "Modern Semiconductor Devices for Integrated Circuits", 1st Ed., Prentice Ha**l**.

Reference Books:

R1. Belty Prince, "Semiconductor Memory Design Handbook".

MIXED AND RF VLSI LAB

Subject Code : PGEC2P1022 **L T P C**

I Year/ II Semester **0 0 3 1.5**

Prerequisites

- Analog IC Design Lab

EXPERIMENTS

1. Fully compensated op-amp with resistor and miller compensation
2. High speed comparator design
3. Data converter
4. Switched capacitor circuits
   i. Parasitic sensitive integrator
   ii. Parasitic insensitive integrator
5. Design of Mixer
6. Design of VCO
7. Design of Low Pass Filter
8. Layouts of All the circuits Designed and Simulated

Laboratory Outcomes : At the end of the course, the students should be able to

LOS	Laboratory outcomes	Bloom's level
LO 1	Explain the necessity of mixed signal systems	II. Understanding
LO 2	Design layout techniques specific to mixed signal IC design	VI. Creating
LO 3	Categorize digital and analog subsystems	IV. Analyzing
LO 4	Design Op-amp compensated against process and temperature variations meeting the mixed signal specifications	VI. Creating
LO 5	Design comparators that can meet the high speed requirements of digital circuitry.	VI. Creating
LO 6	Design a complete mixed signal system that includes efficient data conversion and RF circuits with minimizing switching and phase noise, jitter.	VI. Creating

Mapping of Los to Pos:

POs	LO1	LO2	LO3	LO4	LO5	LO6	LO7	LO8	LO9	LO10	LO11
LO 1				3					3		
LO 2		3	3	3	3						
LO 3				3					3		
LO 4		3	3	3	3		3		3		3
LO 5		3	3	3	3		3		3		3
LO 6		3	3	3	3		3		3		3

PHYSICAL DESIGN LABORATORY

Subject Code: PGEC2P1122 **L T P C**

I Year/ II Semester **0 0 3 1.5**

Prerequisites:

- CAD for VLSI

Laboratory Objective: To give knowledge of VLSI optimization algorithms in c language.

LIST OF EXPERIMENTS:

CYCLE 1

1. Graph algorithms
2. Graph search algorithms
3. Depth first search
4. Breadth first search
5. Spanning tree algorithm
6. Kruskal's algorithm
7. Shortest path algorithm
8. Dijkstra algorithm

CYCLE 2

9. Partitioning algorithms
10. Group migration algorithms
11. Kernighan –Lin algorithm

Laboratory Outcomes: At the end of the course, the students should be able to

LOs	Laboratory outcomes	Bloom's level
LO 1	Apply the constraints posed by the VLSI fabrication technology to design automation tools	III. Applying
LO 2	Design algorithms to meet the critical design parameters	VI. Creating
LO 3	Design layout optimization techniques and map them to the algorithms	VI. Creating
LO 4	Develop proto-type EDA tool and test its efficiency	III. Applying

Mapping of LOs to POs :

POs	LO1	LO2	LO3	LO4	LO5	LO6	LO7	LO8	LO9	LO10	LO11
LO 1		3	3	3	3		3		3		
LO 2			3	3	3		3		3		
LO 3		3	3	3	3		3		3		
LO 4			3	3	3		3		3		