# SHRI VISHNU ENGINEERING COLLEGE FOR WOMEN

## (Autonomous)
## Department of Electronics & Communication Engineering
## Vishnupur, Bhimavaram - 534202

# VLSI Laboratory

**Lab-In-Charge** : Dr. M. Sumalatha

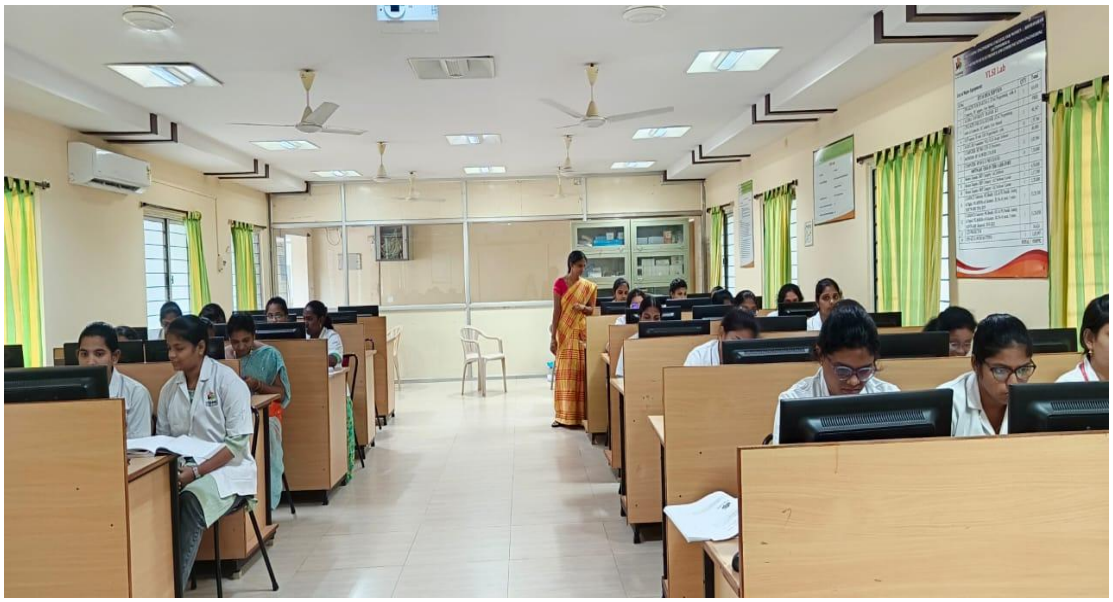
**Lab-Technician** : Mr. P. Chiranjeevi Varma

**Objective:**

VLSI (Very Large-Scale Integration) Laboratory objectives typically focus on providing students or researchers with hands-on experience in designing and testing integrated circuits (ICs) at a high level of complexity and VLSI Laboratory is aimed to bridge the gap between academics and industry based on well-known Cadence Design Systems, Synopsys, Vivado, Semiconductor Design and related fields.

In VLSI Laboratory students can gain knowledge of the complete VLSI design flow, including system specification, architecture design, logic design, circuit design, physical design, and verification and learning to use various design tools (EDA tools) such as Cadence, Synopsys, Vivado or Mentor Graphics for different stages of VLSI design.

The UG and PG programs are designed to give an in-depth training and knowledge in the areas of Application Specific Integrated Circuits (ASIC).



**LAB EQUIPMENT:**

| S. No. | Item Description | Qty |
|---|---|---|
| 1. | Pynq Z2 | 6 |
| 2. | Pmod KYPD: 1 6-buttonKeypad | 6 |
| 3. | Pmod OLEDrgb: 96 x 64 RGBOLED Display Pmod | 6 |
| 4. | Pmod DA2: Two 12-bit *DIA* Outputs | 6 |
| 5. | Pmod TPH2 : 12-pin Test Point Header | 40 |
| 6. | Boolean Board | 16 |
| 7. | Urbana Board | 2 |
| 8. | Arty A7-100T | 1 |
| | USB cable | 1 |
| 9. | Kria KR-260 | 1 |
| 10. | Kria KV (Video) | 1 |
| | HW-BACCP01-SK-G | 1 |
| 11. | Pynq ZU | 1 |
| 12. | Zynq UltraSca le+ MPSoCZCUI 04 | 1 |
| 13. | UEF-VIV ADO-ENTER -25 (2 bundles) | 1 |
| 14. | UEF-MATSIM-ADDON-25 (2 bundles) | 1 |
| 15. | Synopsis | 2 |
| 16. | CADENCE | 2 |
| 17. | Siemens EDA | 1 |
| 18. | Embedded Development Kit | 1 |
| 19. | IOT Applications | 1 |
| 20. | Software Xilinx Vivado ML Edition (50 users) | 1 |
| 21. | FPGA kits for SPARTAN-ll | 1 |
| 22. | ALTERA University Trainer Kit | 1 |

| | | |
|---|---|---|
| 23. | CPLD kits for COOL RUNNER | 5 |
| 24. | XUP spartan 3E with USB Programmable cable | 10 |
| 25. | XLINX ISE Foundation V82i VLSI Design Software | 1 |
| 26. | Computer: HP PRO 3330 -I3 Processors, Monitor: HP 18.5wide Color | 12 |
| 27. | COMPUTER: HP280 G I3 PROCESSORS | 24 |
| 28. | MULTIVENDER UNIVERSAL DEMO BOARD | 2 |
| 29. | CADENCE University PG Bundle (UG & PG Bundle Analog & Digital FE&BE) No of Licenses: 20, No of years: 3 years-SOFTWARE | 1 |
| 30. | LCD Projector | 1 |
| 31. | UPS-6KVA with Batteries | 1 |

# List of Publications:

1. Jaiswal, N.K., Ramakrishnan, V.N. "A Vertical GaN Split Gate Trench MOSFET Device with Reduced Switching Energy Losses". In: Singh, R., Singh, M., Kapoor, A. (eds) The Physics of Semiconductor Devices, Springer Proceedings in Physics, vol 306. Springer, Singapore. https://doi.org/10.1007/978-981-97-1571-8_41. 2024.

2. Venkata Ganeswara Rao Maddipati., Ramanjaneyulu, N., Pydi, B. et al. "Enhancing Performance of Dual-Gate FinFET with High-K Gate Dielectric Materials in 5 nm Technology: A Simulation Study". Transactions on Electrical and Electronic Materials. 24, 557–569 , DOI: 10.1007/s42341-023-00473-5, 2023.

3. Prasad, D.D. et al. "Full Swing Logic Based Full Adder for Low Power Applications". In: Pareek, P., Gupta, N., Reis, M.J.C.S. (eds) Cognitive Computing and Cyber Physical Systems . Lecture Notes of the Institute for Computer Sciences, Social Informatics and Telecommunications Engineering, vol 537. Springer, Cham. https://doi.org/10.1007/978-3-031-48891-7_2,2023.

4. Venkata Ganeswara Rao Maddipati, Navya Sri Mahitha G, Bhavya Sai D, Soudha Basheera Bhanu B, Pravallika G, Gowtham Maddipati "High Performance VLSI Architecure for Real Tieme Edge Detection " in Recent Advances in Computational Intelligence and Communication , DOI: 10.1109/ICACIC59454.2023.10435054, 2023.

5. Venkata Ganeswara Rao Maddipati, Kumar PR, Balaji T. "A High Performance Dual Stage Face Detection Algorithm Implementation using FPGA Chip and DSP Processor", in Journal of Information Systems and Telecommunication (JIST). Oct;4(40):241, DOI: 10.52547/jist.31803.10.40.241,2022.

6. Subbulakshmi N, Pradeep M, Kumar PS, Rajeswaran N. "Floorplanning for thermal consideration: Slicing with low power on field programmable gate array" Measurement Sensors.;24:100491, DOI: 10.1016/j.measen.2022.100491 ,2022.

7. G. R. L. V. N. S. Raju, T. N. Nikitha, G. C. Ram, U. G. Chary, J. N. V. Vardhan and J. D. Kumar, "Area Optimised Efficient Multiplication Using Modified Round Square Approximation," IEEE Integrated Circuits and Communication Systems, Raichur, India, , pp. 1-5, DOI: 10.1109/ICICACS57338.2023.10099920, 2023.